UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SHIGENOBU MAEDA and YASUO YAMAGUCHI

Appeal No. 2005-2685
Application No. 09/176,315

HEARD: December 13, 2005

Before GROSS, BARRY, and SAADAT, *Administrative Patent Judges.*
BARRY, *Administrative Patent Judge.*

A patent examiner rejected claims 1-5 and 18. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse.

I. BACKGROUND

The invention at issue on appeal is a semiconductive device having a metal oxide semiconductor ("MOS") transistor formed on a semiconductor-on-insulator ("SOI") substrate. (Spec. at 1.) Figure 21 of the appellants' specification shows an N-type MOS transistor having an SOI structure in which a body portion is floating. (*Id.* at 2.) More specifically, an SOI layer 3 is formed on a buried oxide film 2, which is formed on a supporting substrate 1. (*Id.* at 2-3.) An N-type drain region 11 and an N-type source

region 12 are formed in the SOI layer. A P-type region of the SOI layer, which includes a body region between the drain and source regions, is defined as a body portion 13. A gate oxide film 10 is formed on the body portion between the drain and source regions, and a gate electrode 6 is formed on the gate oxide film. If the potential of the body portion is not fixed, a body potential ("BV") is changed by the influences of signals flowing through the drain and source regions, which changes the operating speed ("VC") of the MOS transistor as shown in Figure 22 of the specification. (*Id.* at 3.)

Accordingly, the appellants' invention comprises two methods for determining a layout pattern for a MOS transistor. The first method determines a transistor layout pattern based on an operating clock frequency ("f") of at least 500 MHZ. More specifically, the layout pattern must satisfy the expression $R \cdot C \cdot f < 1$. (Appeal Br. at 2.) In this expression, R represents the resistance of a fixed potential transmission path extending from a body contact on a body portion of the MOS transistor to a body region that is between an N-type source region and an N-type drain region that are both formed in an SOI layer of the MOS transistor and C represents the gate capacitance of the MOS transistor. (*Id.* at 2-3.)

The second method determines a transistor layout pattern based on a signal propagation time ("td") required for the MOS transistor that is less than 50 ps. More specifically, the layout pattern must satisfy the expression (R•C)/td<1. (*Id.* at 3.)

A further understanding of the invention can be achieved by reading the following claims.

> 1. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an S0I layer, said MOS transistor being operated based on a predetermined clock,
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> said MOS transistor comprising:
>
> a first semiconductor region of a first conductivity type and selectively formed in said SOI layer,
>
> a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;
>
> a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;
>
> a gate electrode formed on a gate oxide film formed on said body region; and at least one body contact electrically connected to said body portion and receiving a fixed potential,
>
> said method comprising the steps of:
>
> (a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression $R \cdot C \cdot f < 1$ where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ.

2. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer,

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; said gate electrode being electrically connected to said body portion; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing a signal propagation delay time required for said MOS transistor; and

(b) determining a layout pattern of said MOS transistor based on said signal propagation delay time,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression $(R \cdot C)/td < 1$ where

C = the gate capacitance of said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

td = signal propagation delay time (s) required for said MOS transistor, and

$td \leq 50$ ps.

Claims 1-5 and 18 stand rejected under 35 U.S.C. § 103(a) as obvious over *High-speed 0.5 μm SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications* ("Iwamatsu"); U.S. Patent No. 5,767,549 ("Chen"); Japanese Patent Application 06224302 ("Agari"); U.S. Patent No. 5,023,488 ("Gunning"); U.S. Patent No. 3,855,610 ("Masuda"); and U.S. Patent No. 4,899,202 ("Blake").

II. OPINION

Rather than reiterate the positions of the examiner or the appellants *in toto*, we focus on a point of contention therebetween. The examiner admits that "Iwamatsu et al. does not specifically discuss RC time constants," (Examiner's Answer at 6), and "that the Chen teaching applies **to the total capacitance** that contributes to the RC time constant of the current path within the body link." (*Id.* at 7 (emphasis added).) She explains that "the Gunning reference is relied upon to teach that the discharge of the gate capacitance through the substrate, specifically, is known," (*id.* at 8); that "Masuda et al. teaches at column 2, lines 40-47, various known capacitances associated with a MOS transistor," (*id.*), "[i]n particular, gate-to-substrate capacitance," (*id.*); and that "the Agari reference teaches that the total RC time constant for any current path is the result of all contributing RC time constants." (*Id.*) The examiner then draws the following conclusion.

> [I]t would have been obvious to design a transistor having an RC time constant contribution from the gate capacitance to be less than a desired value determined by the frequency of operation, because the current path through the body link is known, the discharge of the gate capacitance through this current path is known, the association of this current path with a total RC time constant is known, the contribution of each known capacitance to the total RC time constant is known, and because the

> minimization of RC time constant based on desired operating frequency is known.

(*Id.*) The appellants make the following argument.

> [T]he mere indication by Gunning of "drain-side capacitances," "source-side capacitances" and "gate-substrate capacitance" and that of Masuda as to "C_{GP}," "C_{GS}," and "C_{PS}" do change the simple fact that the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) includes no such capacitance components, otherwise known or not. . . .

(Appeal Br. at 17.) In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claim at issue to determine their scope. Second, we determine whether the construed claims would have been obvious.

1. CLAIM CONSTRUCTION

"Analysis begins with a key legal question — *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Here, independent claim 1 recites in pertinent part the following limitations: "determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock, wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression R•C•f<1 where C = the gate capacitance said MOS transistor." Similarly, independent claim 2 recites

in pertinent part the following limitations: "determining a layout pattern of said MOS transistor based on said signal propagation delay time, wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression (R•C)/td < 1 where C = the gate capacitance of said MOS transistor." Accordingly, both independent claims require using the gate capacitance of a MOS transistor in determining a layout pattern thereof.

2. OBVIOUSNESS DETERMINATION

"Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious." *Ex Parte Massingill*, No. 2003-0506, 2004 WL 1646421, at *3 (Bd.Pat.App & Int. May 20, 2004). "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "'A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.'" *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, as aforementioned, the examiner admits "that the Chen teaching applies to the total capacitance that contributes to the RC time constant of the current path within the body link." (Examiner's Answer at 7.) It is uncontested that Gunning "teach[es] that the discharge of the gate capacitance through the substrate, specifically, is known," (*id.* at 8); that "Masuda et al. teaches . . . gate-to-substrate capacitance," (*id.*); and that "Agari . . . teaches that the total RC time constant for any current path is the result of all contributing RC time constants." (*Id.*) Because none of the references uses the gate capacitance of a MOS transistor to determine a layout pattern thereof, however, we are unpersuaded that the references would have suggested using the gate capacitance of a MOS transistor rather than the total capacitance thereof, which is what Chen teaches, in determining a layout pattern of the MOS transistor.

Furthermore, the examiner does not allege, let alone show, that the addition of Blake cures the aforementioned deficiency of Iwamatsu, Chen, Agari, Gunning, and Masuda. Absent a teaching or suggestion of using the gate capacitance of a MOS transistor in determining a layout pattern thereof, we are unpersuaded of a *prima facie* case of obviousness. Therefore, we reverse the obviousness rejection of claims 1 and 2 and of claims 3-16 and 18, which depend therefrom.

III. CONCLUSION

In summary, the rejection of claims 1-5 and 18 under § 103(a) is reversed.

REVERSED

ANITA PELLMAN GROSS
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

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